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A CASSETTE TAPE RECORDER/READER INTERFACE FOR MICROPROCESSORS.(U)
NOV 78 P FERRAROTTO

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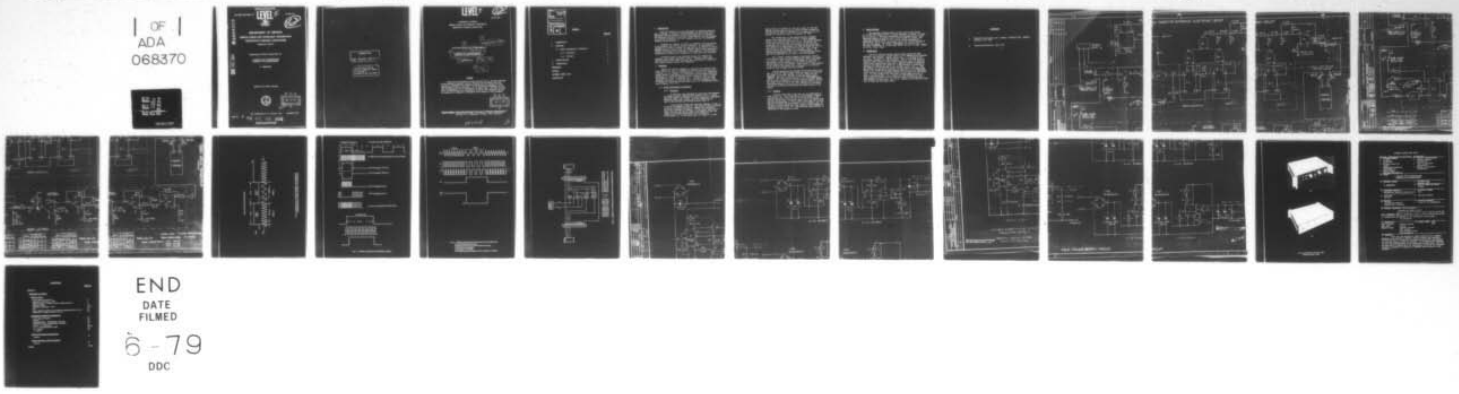

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Aerodynamics Technical Memorandum 311

A CASSETTE TAPE RECORDER/READER INTERFACE FOR MICROPROCESSORS

P. FERRAROTTO

Approved for Public Release.

November 1978.

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6 A CASSETTE TAPE RECORDER/READER INTERFACE FOR MICROPROCESSORS

10 P. FERRAROTTO

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12 31p.

SUMMARY

This unit was designed to enable digital data or computer programs to be recorded on domestic quality cassette tape recorders, and thus provide an inexpensive and convenient method for the exchange or long-term storage of data or programs. It was specifically designed for use with microprocessors as an alternative to paper tape. This unit has been built to conform with the requirements of the RS. 232 standard, and may be connected to terminals or computers which conform to this standard.

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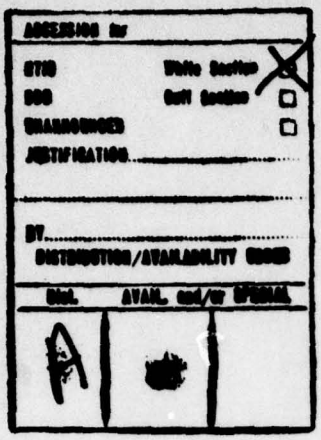

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1. INTRODUCTION

With the growing use of microprocessors as complete systems or part of systems, a method of storing programs and data which is more convenient than the generally used punched paper tape is required. The interface described in this memo. allows digital data and programs to be stored on magnetic tape using ordinary low cost, low bandwidth cassette recorder/readers.

Programs are compiled as usual by a computer, and then written on the cassette tape via the cassette interface. If the program is required to be loaded or edited (at some time in the future), it can be replayed from the cassette tape into computer memory where execution or editing of the program is performed in the normal way. The unit uses conventional circuits and is inexpensive to build and easy to operate.

A review of many of the published Kansas City designs was conducted (for example references 1 and 2). However, none of the existing designs were judged to fulfil the requirements of simplicity while using in-house stores stock components.

2. OPERATION

Serial data from the computer is converted into either of two tones, 2400 Hz or 1200 Hz, depending on whether the serial data bit is a logical '1' or a logical '0' respectively. The two tone frequencies chosen conform to the Kansas City standard recording format which was formulated at a symposium sponsored by U.S. Magazine "Byte" in Kansas City Missouri, U.S.A., in November 1975. Recorded on cassette tape therefore, are bursts of these two tones. The data recorded on tape is decoded by converting the particular tone to its corresponding logic level (logical '0' or '1').

2.2 Detail Description of Operation

2.2.1 Recording

In this unit, the recording of serial data from terminal or computer employs Frequency Shift Keying (F.S.K.). Serial data from computer or terminal is first converted to Transistor-Transistor-Logic (TTL) levels, since TTL components are used in the encoding and decoding circuits (Fig. 1).

A free running square wave generator (package 'C' Fig. 1) is set at a frequency of 2400 Hz. The output of this oscillator is fed to the encode electronics together with the serial data from a computer or terminal. If the serial data is at a logic 1 at TP4, the 2400 Hz square wave appears at TP5, the output of the encode electronics, for the duration of the logic '1'. If the serial data is a logic '0' at TP4,

then $\bar{Q}$ (Pin 8) of package 'F' will be at logic "1" and this enables a square wave of 1200 Hz (which has been produced by the division of 2400 Hz by package 'F') to appear at pin 5 of package 'B' and hence at pin 11 of package 'B' (TP5).

The encoded data is then passed through a bandpass filter with a pass band gain of unity, a centre frequency 1600 Hz, and a quality factor (Q) of 1.3. The centre frequency is set such that for either tone (1200 Hz or 2400 Hz) the attenuation is the same and at the output of the filter both tones should be of approximately the same amplitude but this is not critical to the functioning of the unit. Fig. 2 shows typical serial data at output of the bandpass filter. An attenuating potentiometer VR1 (Fig. 1) is provided for adjustment of the amplitude at the input to the tape recorder.

Fig. 3 shows a timing diagram of the encoder circuit. A 300 Baud data rate has been assumed which gives a bit length of 3.33 msec. When a logic '1' data appears at the input of the encoder, and its duration is 3.33 m.sec., 8 cycles of 2400 Hz square wave are recorded. When a logic '0' data appears at the input of the encoder and its duration is 3.33 m.sec,4 cycles of 1200 Hz square wave are recorded.

Two BNC connectors are provided on the back panel of the unit to which the tape recorder input and output are connected. The output of the tape recorder is usually taken from the "EARPHONE" jack and is connected to the BNC socket marked "REPLAY". The input to the recorder is the "MICROPHONE INPUT" jack and this is connected to the BNC connector marked "RECORD". The volume level setting on the tape recorder should be set to high during replay to allow the input amplifier in the decode electronics to saturate and produce near square pulses at its output.

2.2.2 Playback

The data, read from a tape (Fig. 4a) is conditioned as shown in Fig. 4b. The rising edge of this waveform triggers a monostable with a duty cycle of 75% of the period of the 2400 Hz. square wave. The signal shown in Fig. 4c results from the $\bar{Q}$ of the monostable. This is used as the clock of a D-flip-flop which decodes the data present on its D terminal, Fig. 4d. The data, correctly phased and level shifted to suit computer or terminal, is shown in Fig. 4c. Light emitting diodes provide an indication of the presence of data.

3. POWER SUPPLIES

The programme recorder/reader printed circuit board serial No. 57-318 (R2) requires three (3) power supplies: +12 volts, -12 volts and +5 volts d.c. The power requirements are adequately met by three regulated supplies on printed circuit board serial No. 57-162. All three power supplies shown in Fig. 5 can be current regulated by adjusting R6, R7 on the +5 volt supply, R12 on the +12 volt and R19 on the -12 volt supply. The current requirements are listed in Fig. 1. The power transformer is a Trimax Type TP5785, 18 volt, 1.5 amp., tapped at 15, 12, 9 and 6 volts.

4. CONSTRUCTION

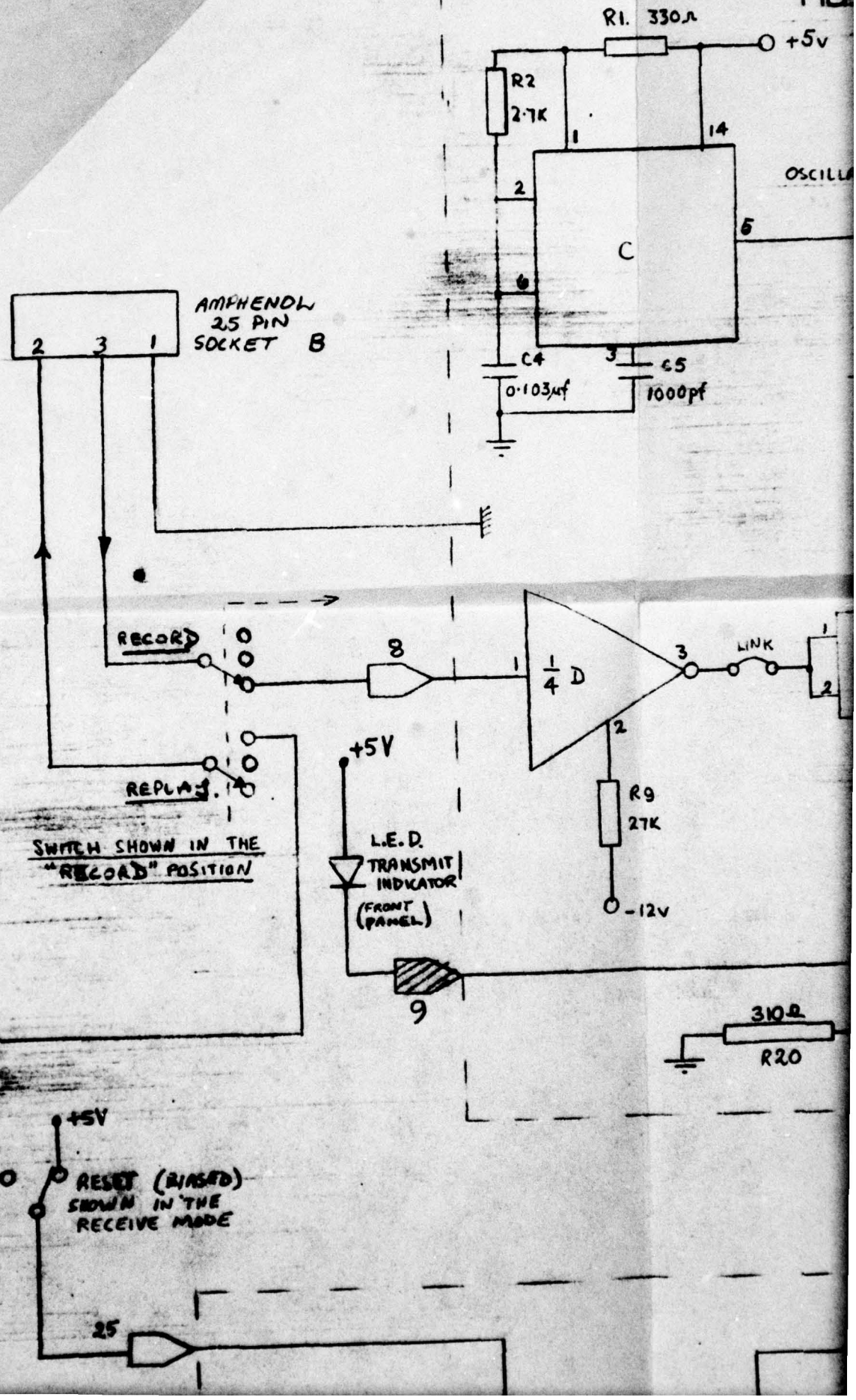
Two A.R.L. M8 size printed circuit boards with 56 pin edge connectors are mounted on captive spacers in an ELMASET 88 mm instrumental case. The 'record', 'replay' switch (Fig. 1) is located on the front panel together with LED indicators. Also on the front panel is located a reset switch, a power on/off switch and a four (4) position switch which interconnects three 25-pin amphenol sockets to which the terminal and computer are connected. A LED. indicator is connected to the output of the D-flip-flop in the decoding circuit, Fig. 1. This LED. flickers to indicate the presence of data when in the replay mode. However, the output of the flip-flop may remain high or low (depending on the last bit of data decoded) although the unit may be in the record mode. To avoid confusion the flip-flop is reset before the unit is used in the record mode. Fig. 6 shows the interconnection of the three amphenol sockets via the 4 position switch and the function of each position of the switch. Fig. 7a is a general view of the unit while Fig. 7b shows the back panel layout.

REFERENCES

1. "MEK 6800 D2 Evaluation Kit II Manual." Motorola Corp., Phoenix Arizona, U.S.A. 1976.

2. "Electronics Australia", April 1977.

FIG.



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REVISION

ALL DIMENSIONS IN .....

TOLERANCES

SCALE

TITLE: PROGRAMME RECORDE

APPROVA

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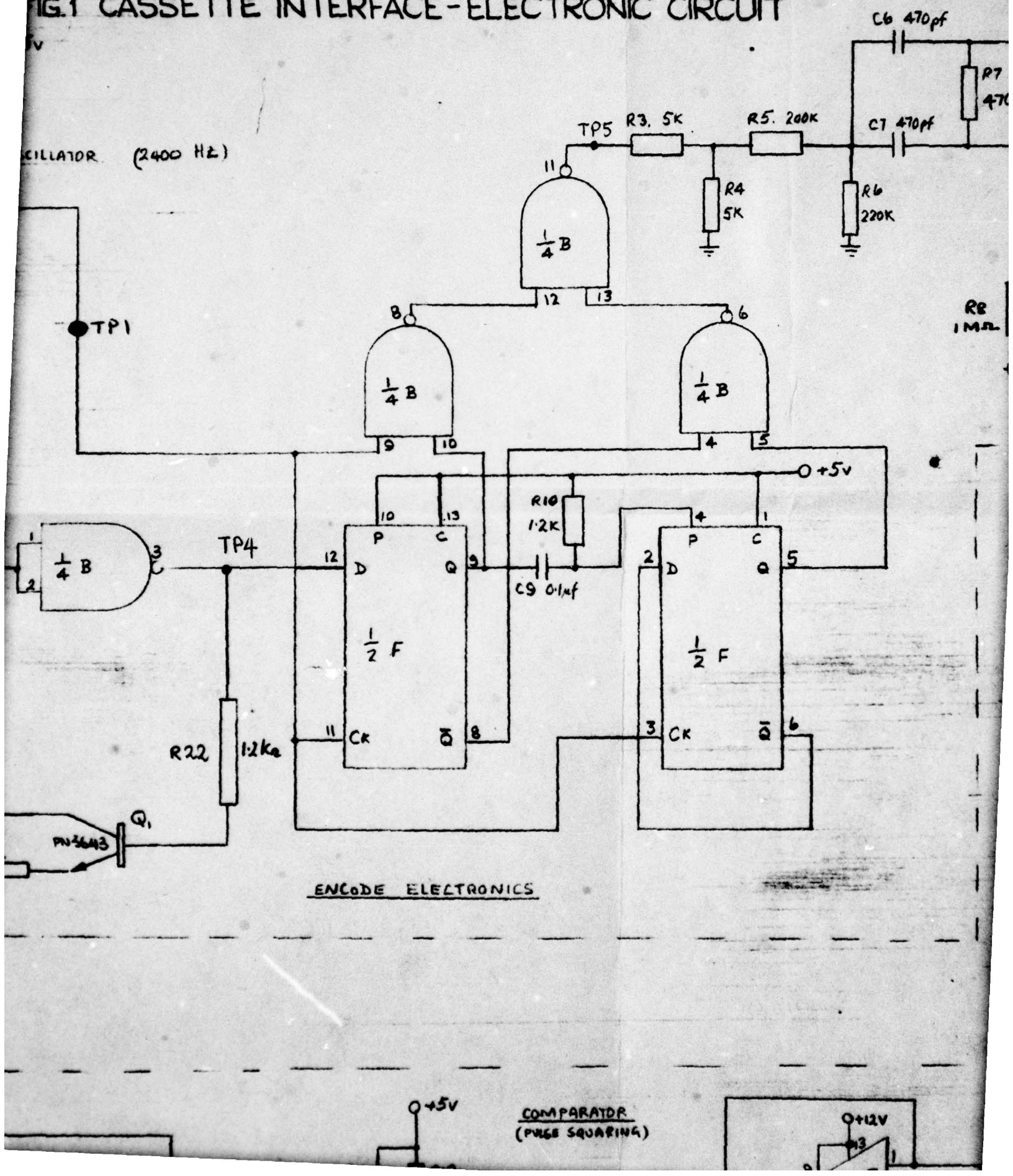
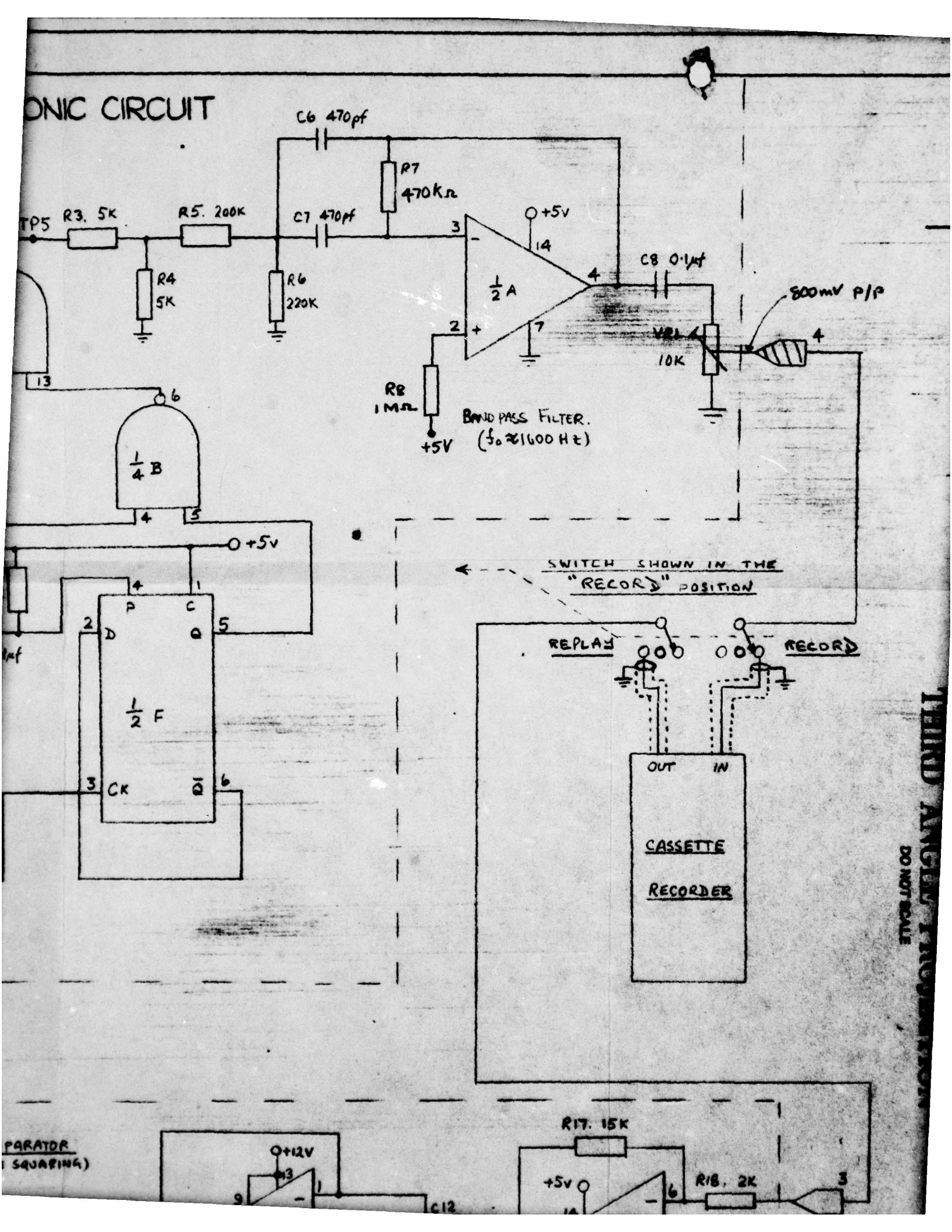
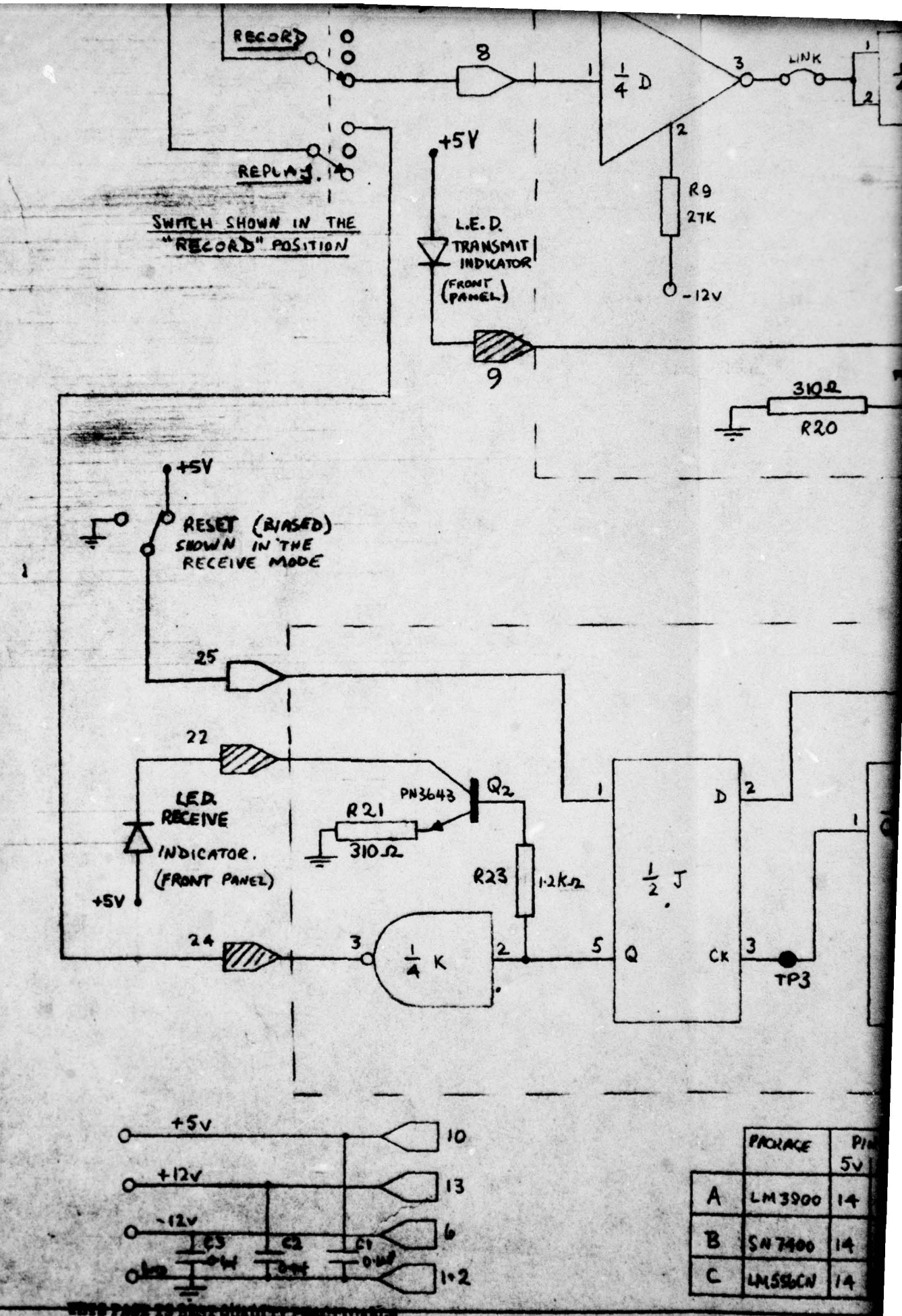
FIG.1 CASSETTE INTERFACE - ELECTRONIC CIRCUIT



ONIC CIRCUIT



THIRD ANGLE PROJECTION
DO NOT SCALE



	PACKAGE	PIN 5V
A	LM3900	14
B	SN7400	14
C	LM556CN	14

TOLERANCES

ALL DIMENSIONS IN

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APPROVAL

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CHECKED

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P.O. No. GEN. ARRGT.

PARTS LIST PL

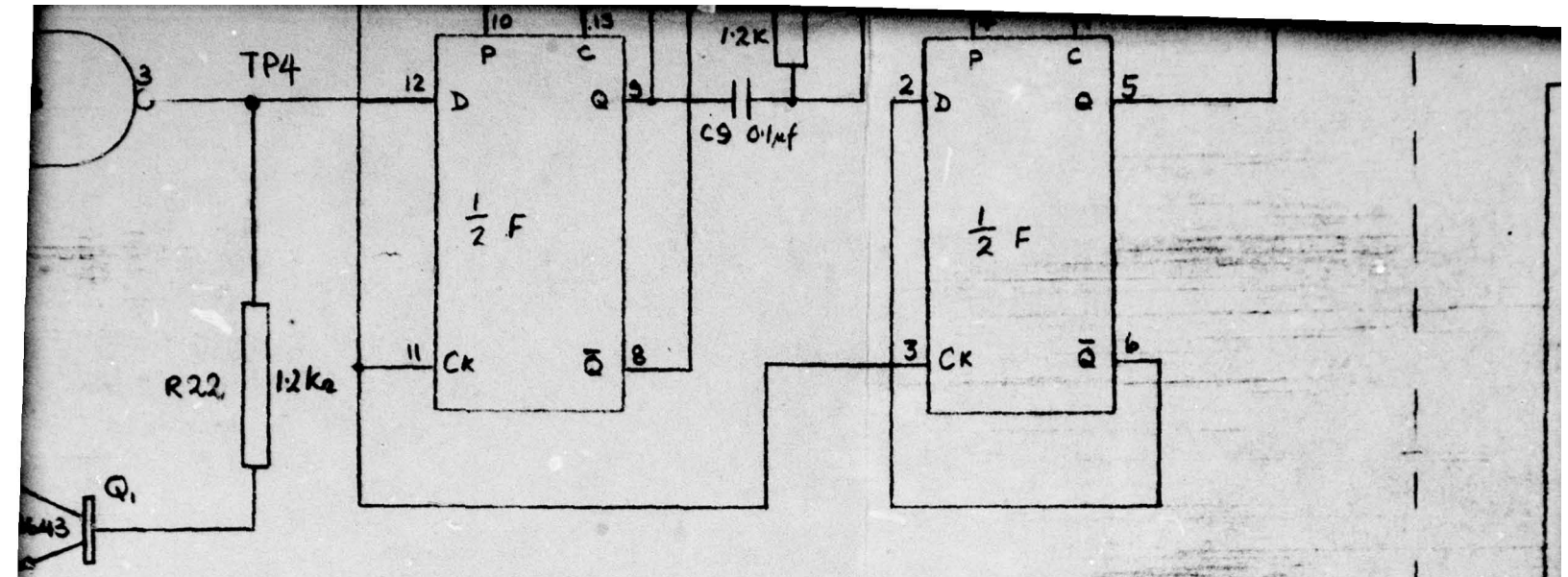
TITLE: PROGRAMME RECORDER/READER

AERONAUTICAL RESEARCH LABORATORIES - AUSTRALIA

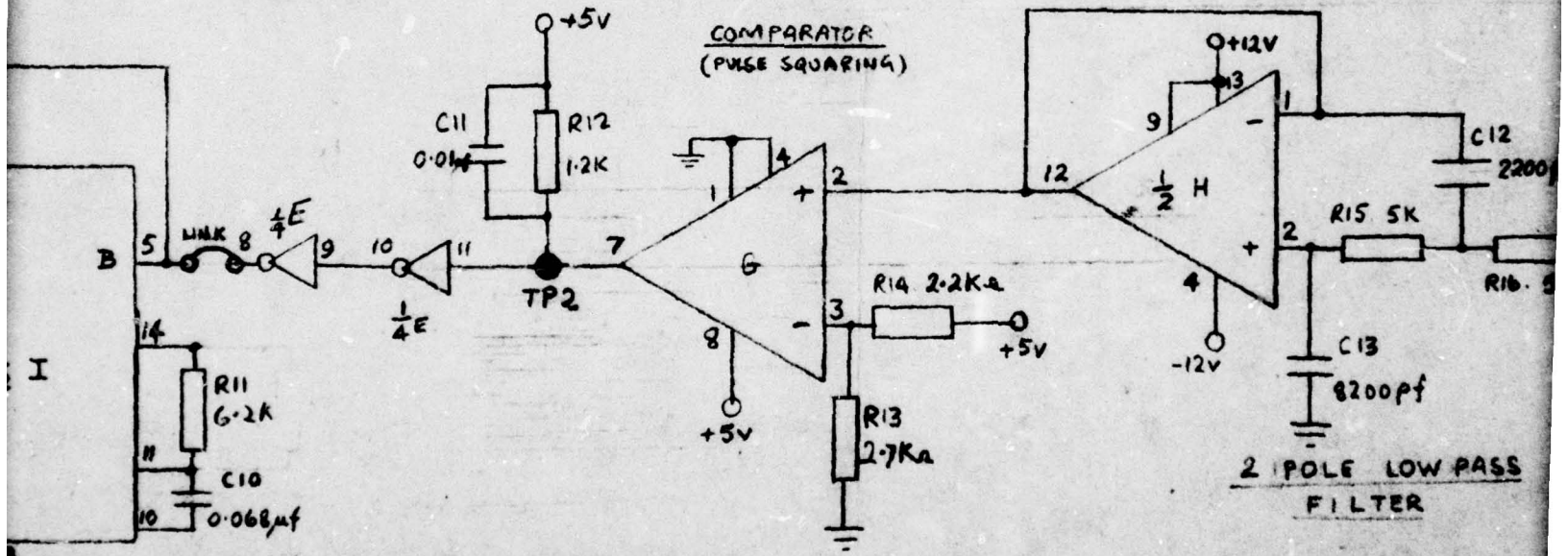
DRG. No.

REVISION No.

A2



ENCODE ELECTRONICS



COMPARATOR (PULSE SQUARING)

2 POLE LOW PASS FILTER

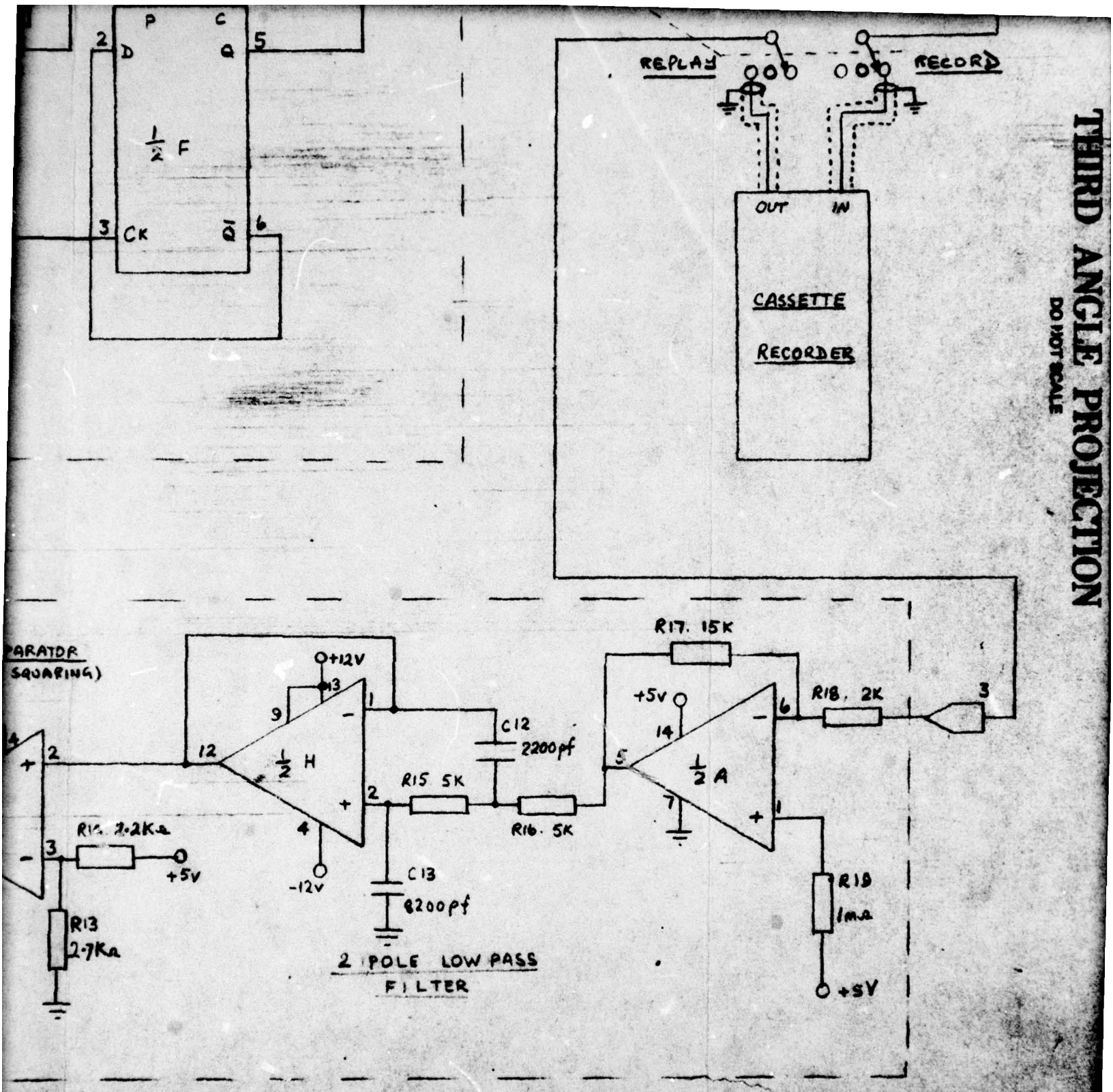
DECODE ELECTRONICS

	PACKAGE	PIN CONNECTIONS +5v	GND	+12v	-12v
D	MC1489	14	7		
E	SN7414	14	7		
F.S.	SN7474	14	7		

	PACKAGE	PIN CONNECTIONS +5v	GND	+12v	-12v
G	LM311D	8	1,4		
H	LM747			9,13	4
I	SN74121	14	7		
K	1488L		7	14	1

BOARD SIZE - M8

POWER REQUIR



THIRD ANGLE PROJECTION

DO NOT SCALE

	PACKAGE	PIN CONNECTIONS +5v	GND	+12v	-12v
G	LM311D	8	1,4		
H	LM747			13	4
I	SN74121	14	7		
K	1488L		7	14	1

BOARD NAME - PROGRAMME RECORDER/REPLAY

BOARD SIZE - M2

BOARD IDENTIFICATION - 57-319 (R2)

POWER REQUIREMENTS — +5 V , 100 mA
+12 V , 20 mA
-12 V , 20 mA

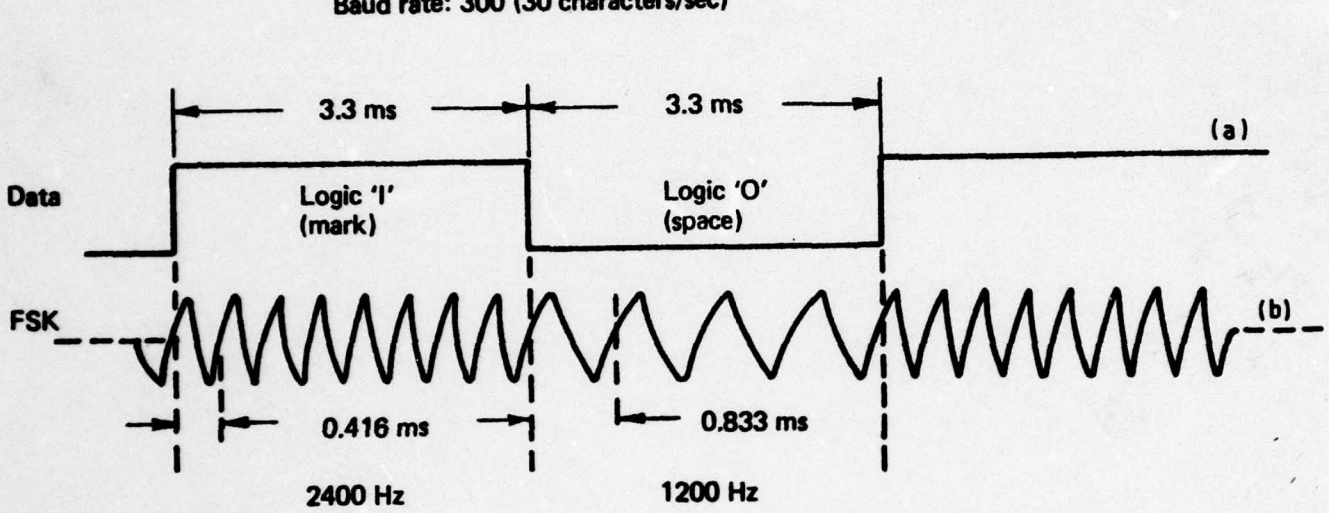


FIG. 2.(a) SERIAL DATA FROM TERMINAL OR COMPUTER
(b) ENCODED DATA (FSK) AS INPUT TO RECORDER

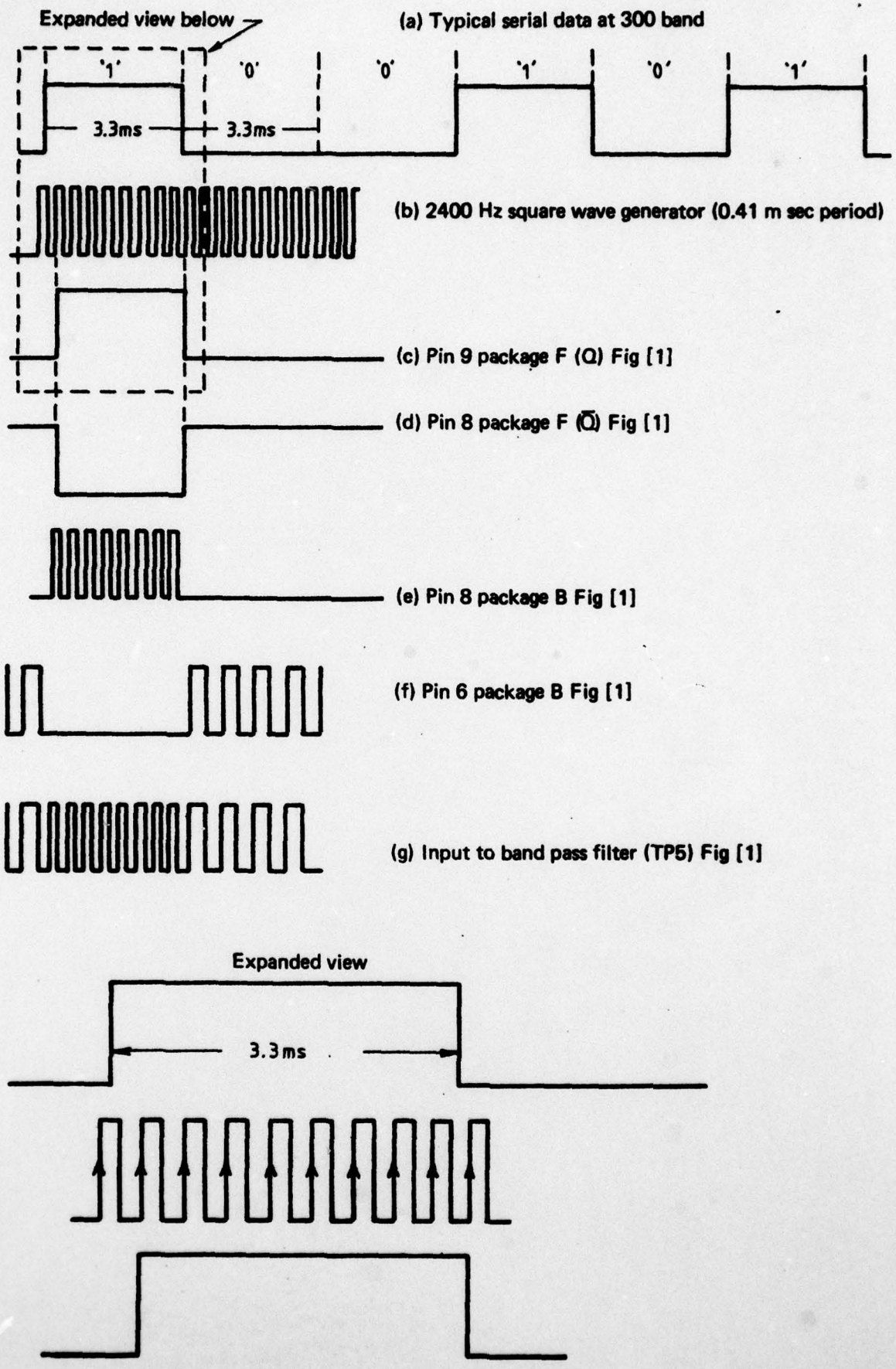


FIG. 3. TIMING DIAGRAM FOR ENCODER CIRCUIT

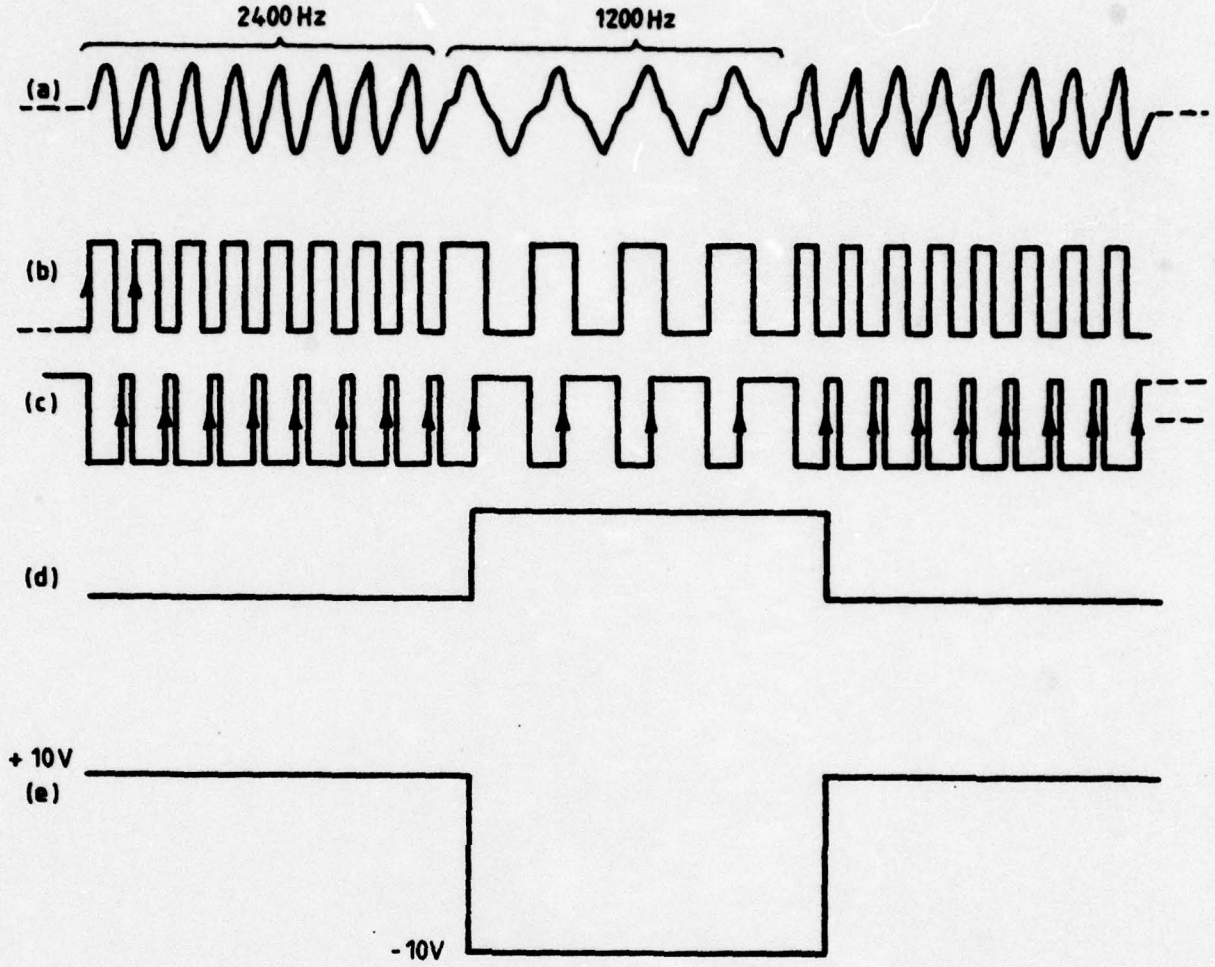
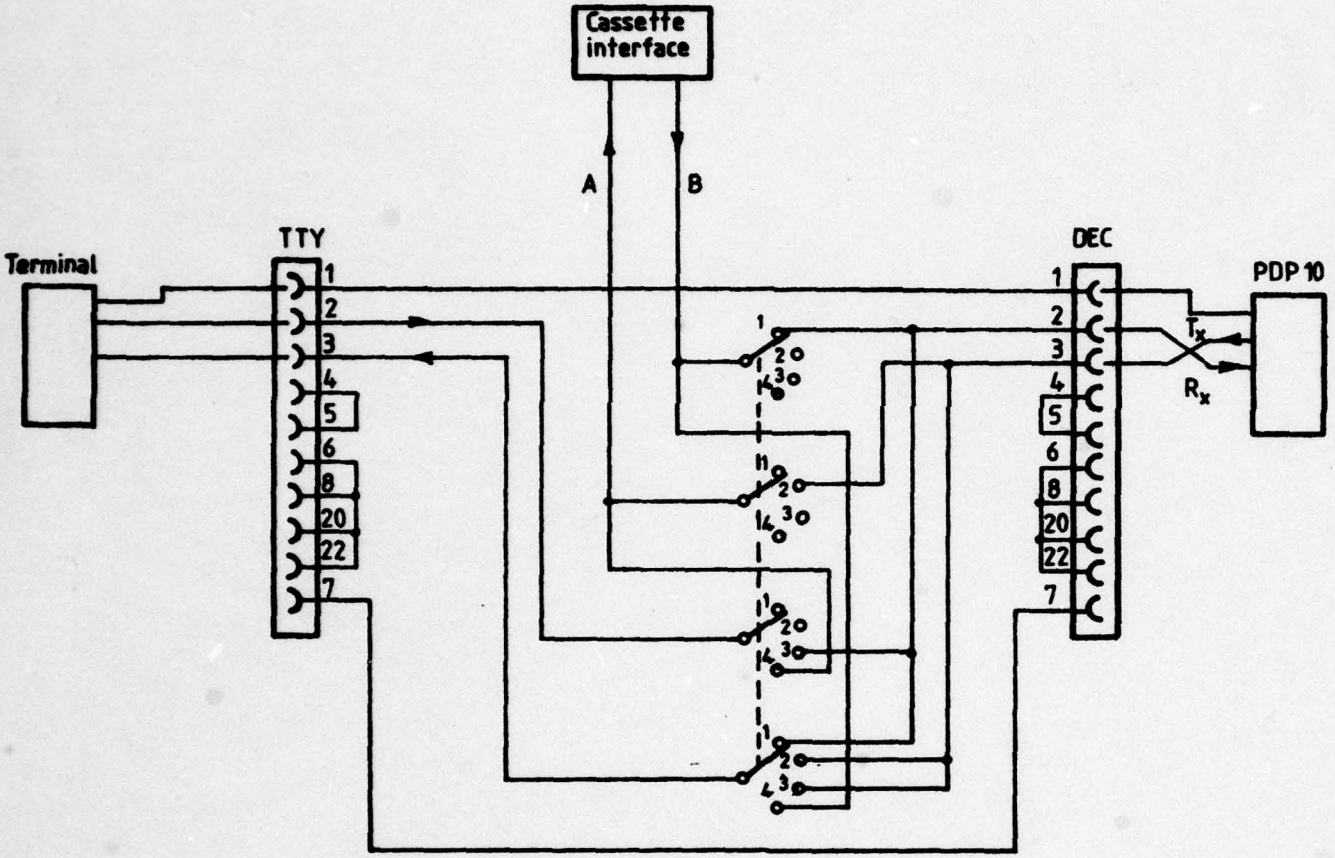


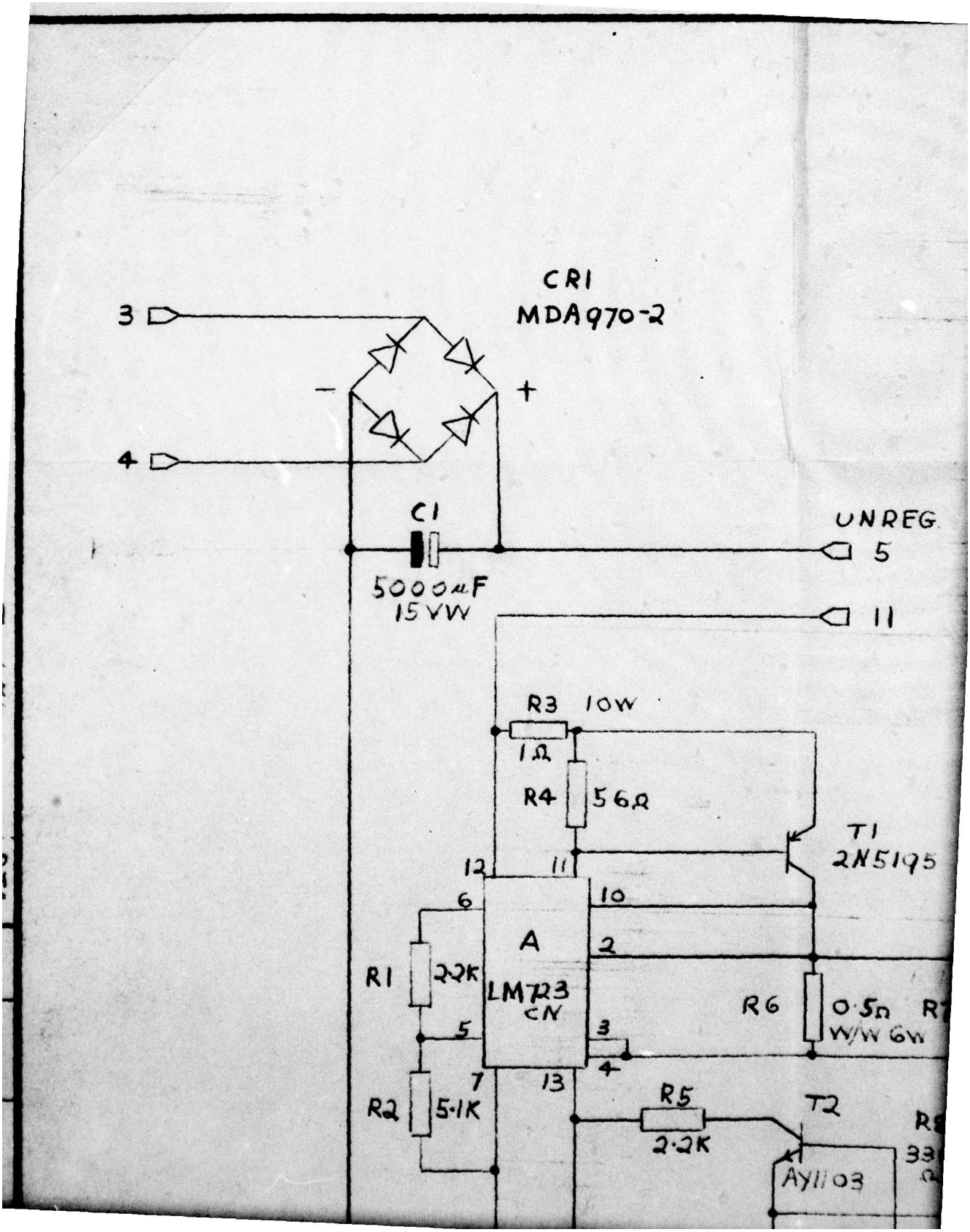
FIG. 4. TIMING DIAGRAM FOR DECODING DATA FROM TAPE

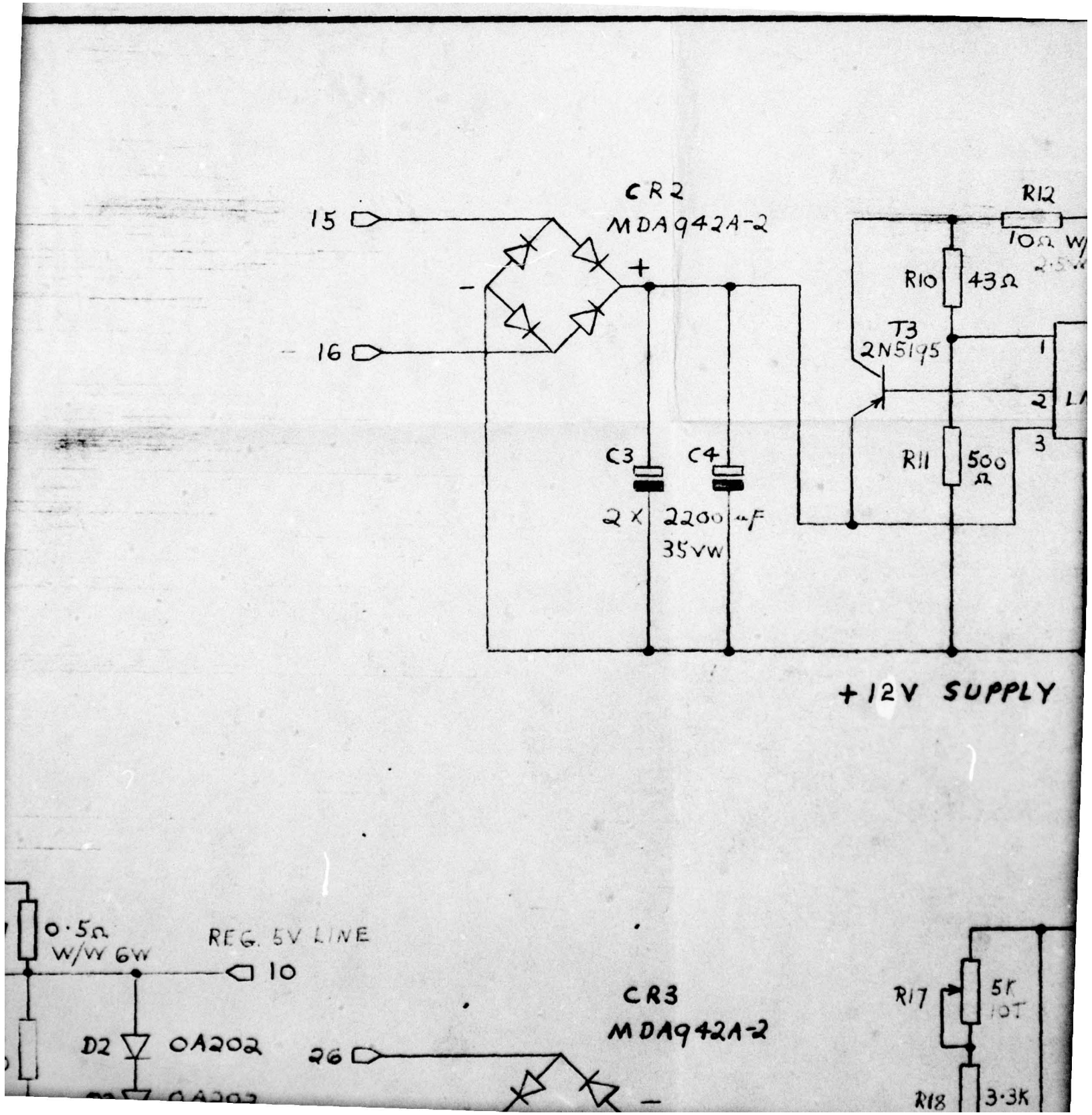
(a) Typical data burst from tape
(b) Data burst after amplifying filtering and squaring
(c) $\bar{Q}$ output of monostable
(d) Q output of D flip-flop
(e) Decoded data level changed to drive computer or terminal.

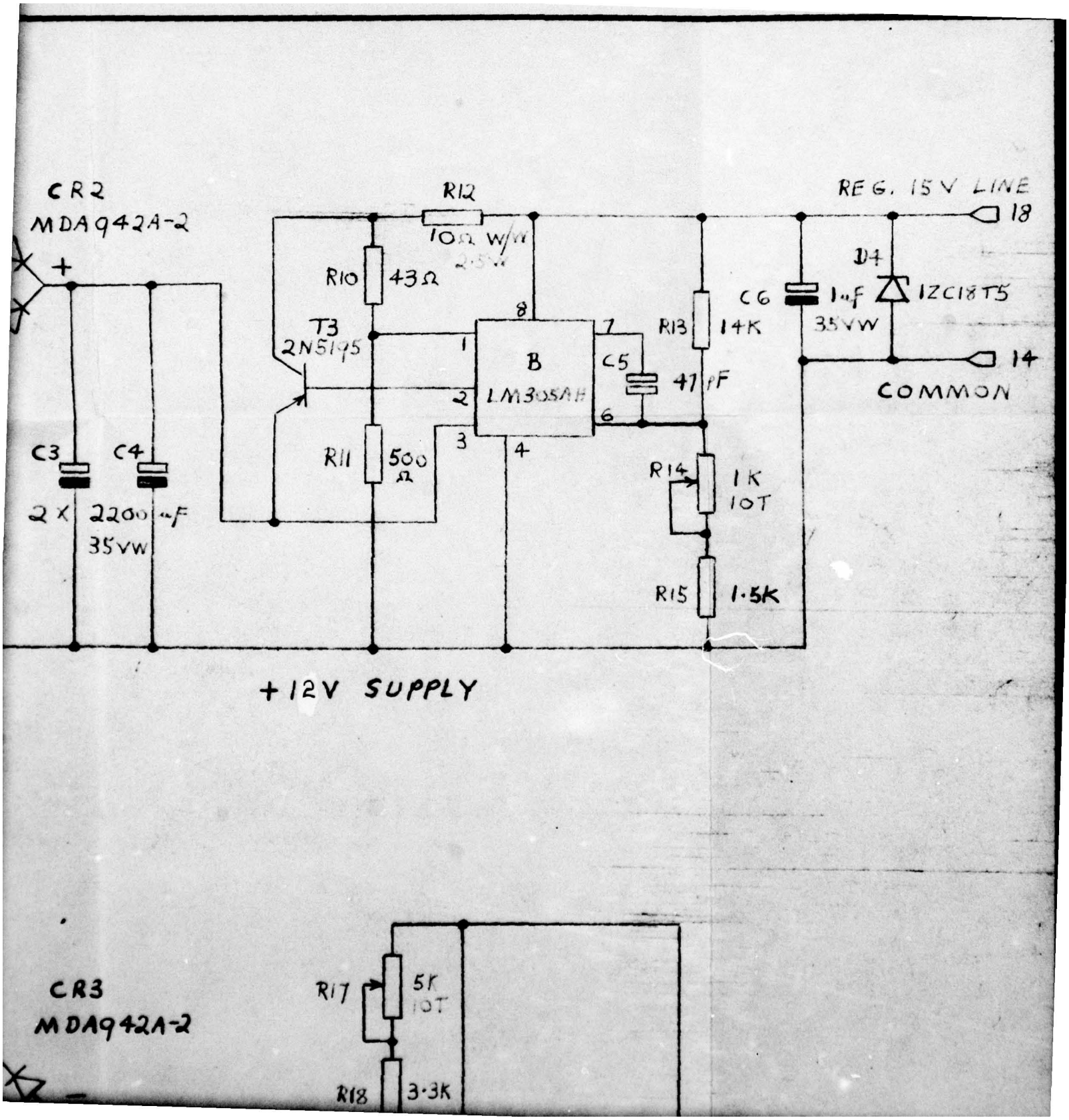


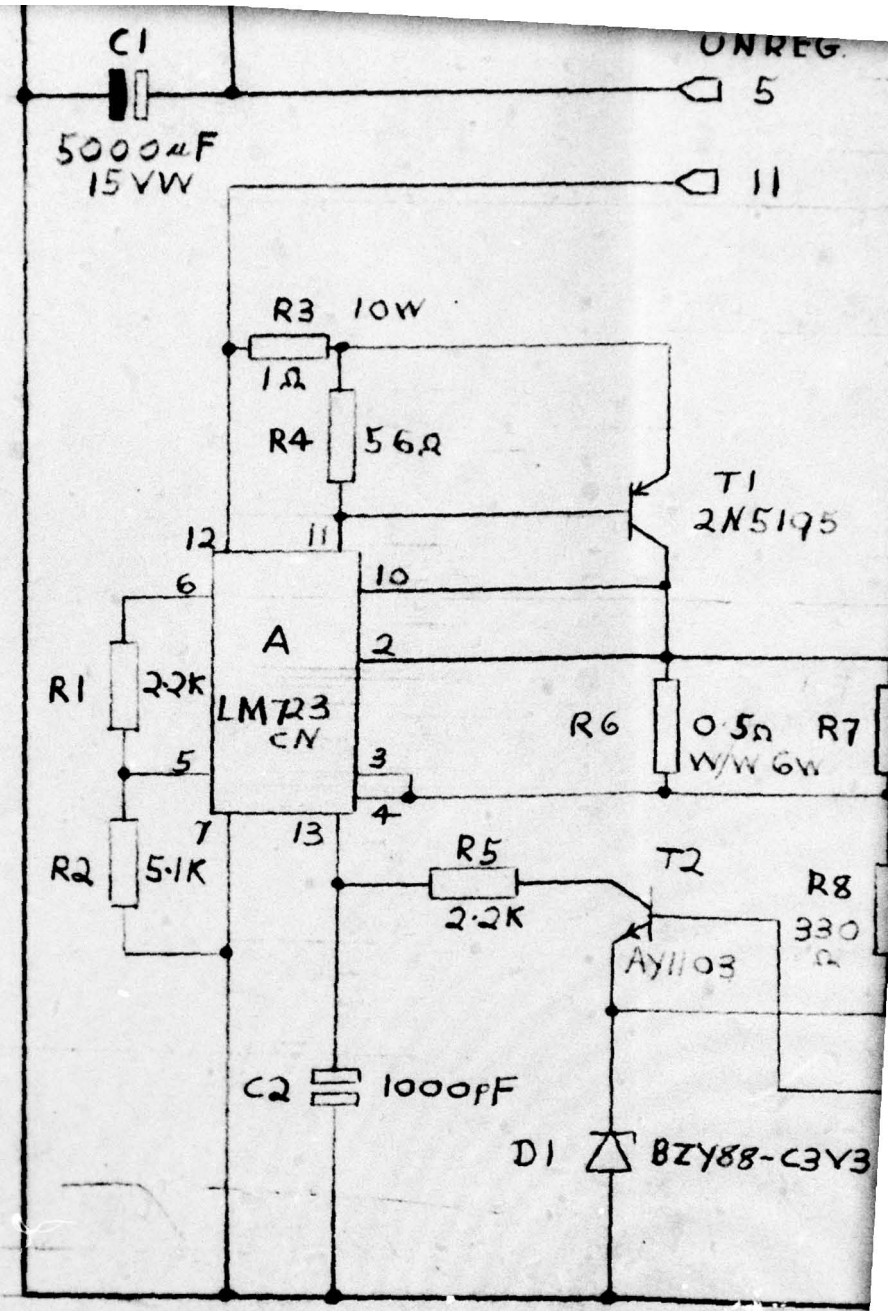
Switch position 1 cassette ⟶ PDP-10 (terminal monitoring)
Switch position 2. PDP-10 ⟶ cassette (terminal monitoring)
Switch position 3 terminal ⟷ PDP-10 (on line)
Switch position 4 cassette ⟶ terminal (terminal not on line)

FIG. 6. CASSETTE INTERFACE 25-PIN SOCKET INTERCONNECTIONS


CR1
MDA970-2
3
4
−
+
C1
5000μF
15VW
UNREG
5
11
R3 10W
1Ω
R4 56Ω
T1
2N5195
12
11
10
6
A
2
R1 22K
LM723
CN
R6 0.5Ω
W/W 6W
5
3
4
7
13
R2 5.1K
R5
2.2K
T2
AY1103
33


CR2
MDA942A-2
15
16
+
−
R12
10Ω W/
R10
43Ω
T3
2N5195
1
2
3
C3
C4
2 X 2200 μF
35VW
R11
500 Ω
+12V SUPPLY
0·5Ω
W/W 6W
REG. 5V LINE
10
D2
OA202
CR3
MDA942A-2
26
−
R17
5K
10T
R18
3·3K


CR2
MDA942A-2
+
C3
C4
2 X 2200 uF
35VW
R12
10Ω W/W
R10
43Ω
T3
2N5195
B
LM305AH
1
2
3
4
6
7
8
C5
47 pF
R11
500 Ω
R13
14K
R14
1K
10T
R15
1.5K
C6
1 uF
35VW
D4
IZC18T5
REG. 15V LINE
18
14
COMMON
+12V SUPPLY
CR3
MDA942A-2
R17
5K
10T
R18
3.3K



+5V 2A SUPPLY

+5 ~~VOLT~~ 2 AMP & DUAL 15 VOLT REGULATED SUPPLIES

PRINTED CIRCUIT BOARD
IDENT No. 57-162

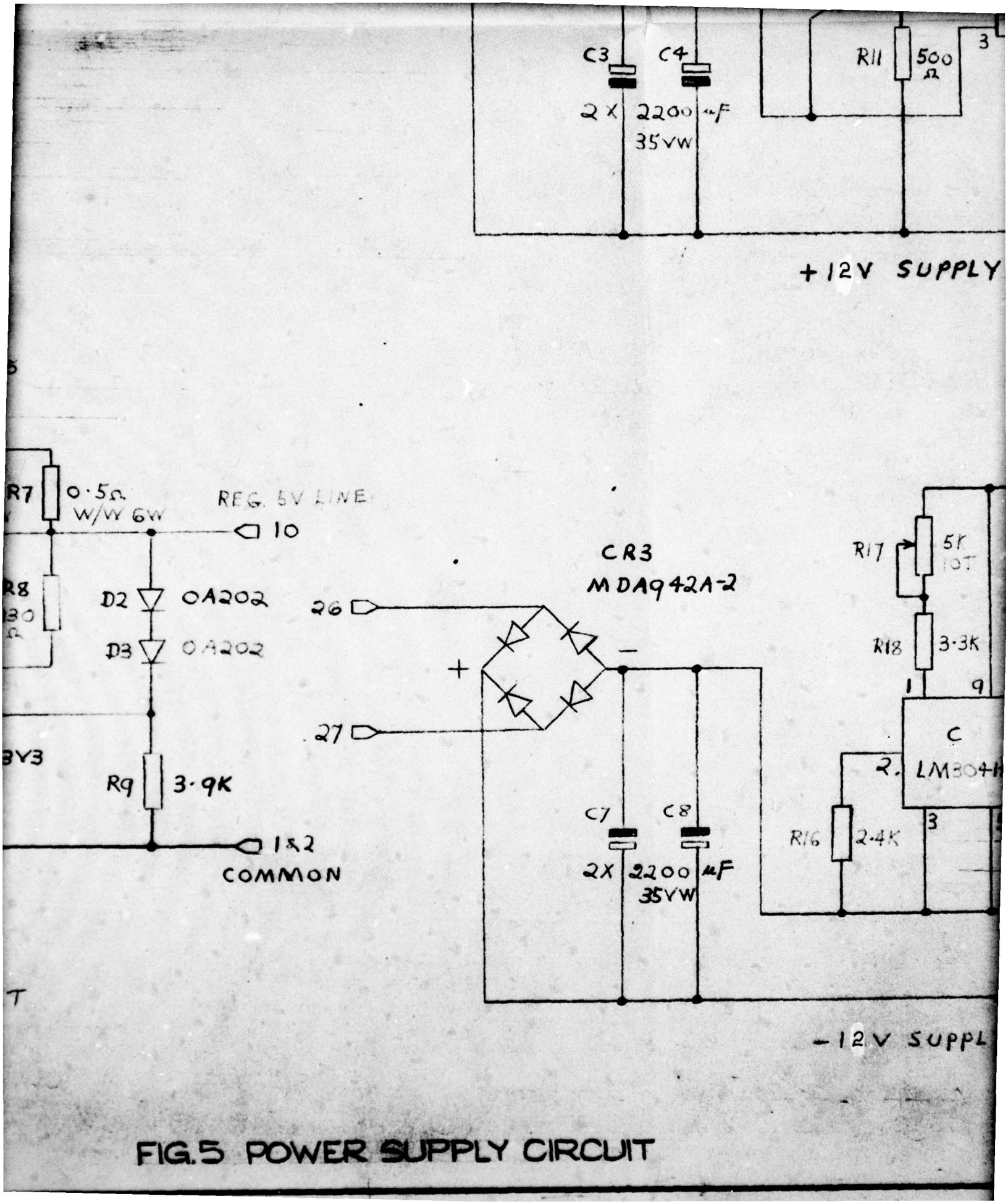
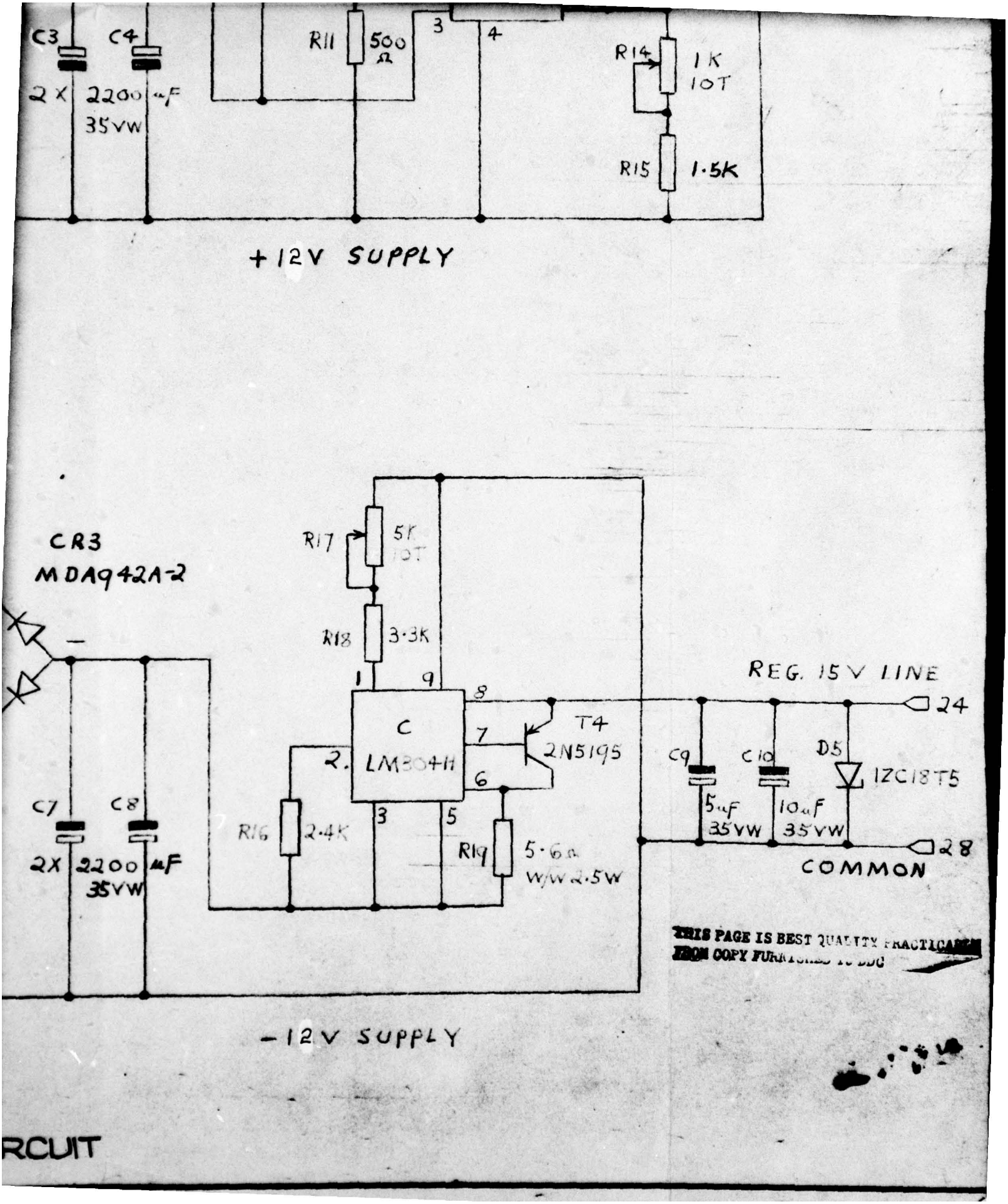
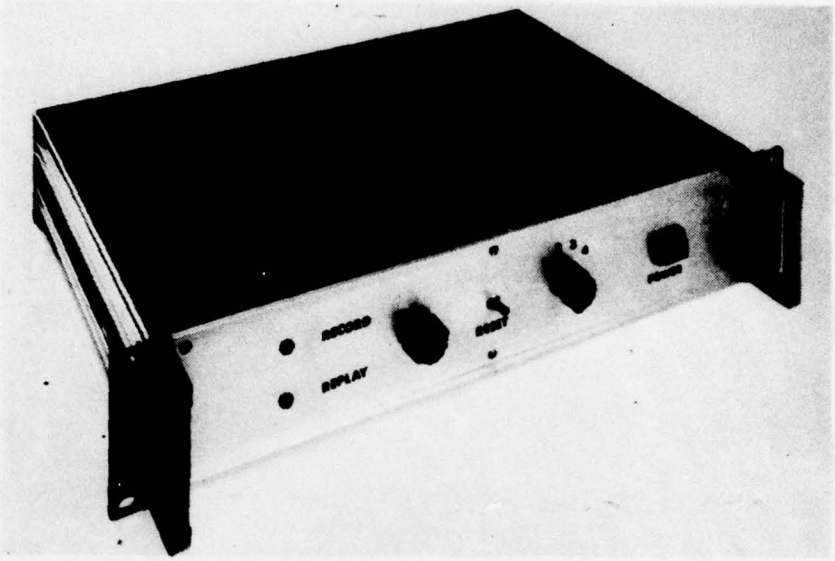


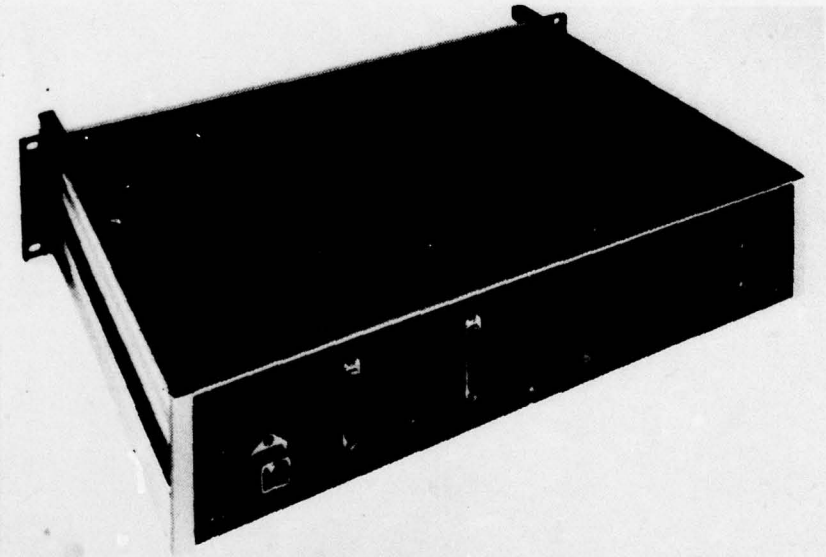
FIG.5 POWER SUPPLY CIRCUIT



RCUIT



(a)



(b)

FIG. 7.(a) GENERAL VIEW OF UNIT
(b) BACK PANEL VIEW

DOCUMENT CONTROL DATA SHEET

Security classification of this page: UNCLASSIFIED

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   b. Document Series and number: Aerodynamics Technical Memorandum 311.
   c. Report Number: ARL-AERO-TECH-MEMO-311

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   a. Complete document: UNCLASSIFIED
   b. Title in isolation: UNCLASSIFIED
   c. Summary in isolation: UNCLASSIFIED

3. TITLE:
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4. PERSONAL AUTHOR:
   P. PERRAROTTO.

5. DOCUMENT DATE:
   November, 1978

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12-0. OVERSEAS: NO | | P.R. | 1 | A | | B | | C | | D | | E |

13. ANNOUNCEMENT LIMITATIONS (of the information on this page):
    No limitation.

14. DESCRIPTORS:
    Tape recorders.
    Data tapes.
    Magnetic tapes.
    Computer storage devices.
    Computer programs.
    Data storage.
    Data storage devices.
    Microprocessors.

15. COSATI CODES: 1403, 0402

16. ABSTRACT:

This unit was designed to enable digital data or computer programs to be recorded on domestic quality cassette tape recorders, and thus provide an inexpensive and convenient method for the exchange or long-term storage of data or programs. It was specifically designed for use with microprocessors as an alternative to paper tape. This unit has been built to conform with the requirements of the RS. 232 standard, and may be connected to terminals or computers which conform to this standard.

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